Beyond CMOS

Ultimate CMOS: High k dielectrics on high carrier mobility semiconductors - accomplishments and challenges

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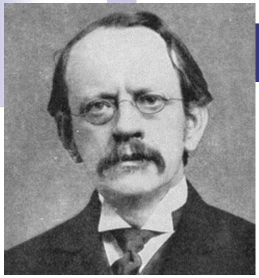
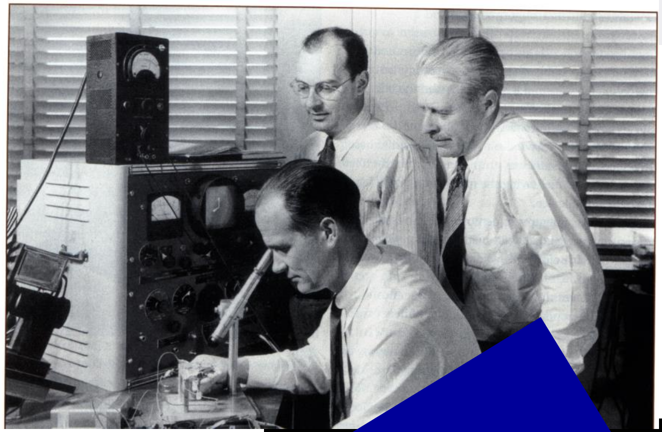


1897 J. J. Thomson discovery of electron - using properties of cathode rays, electron charges

The cathode ray tube (CRT) is a vacuum tube

What next?



1… …sistor

2007 High k + metal gate on Si for 45 n… …32 nm, 2012 22 nm, and 2014 15 nm node. InGaAs, Ge, … 2025?

Quantum Mechanics and Spin!!!

- Mervin Kelly, the then Direc… …ell Labs, had predicted the problem and had already taken ac… …n.
  - Although relays an… …apparently making all things possible in telephony, he had predicted for s… …the low speed of relays and the short life and high power consumption of tubes w… …ntually limit further progress in telephony and other electronic endeavors.
  - In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

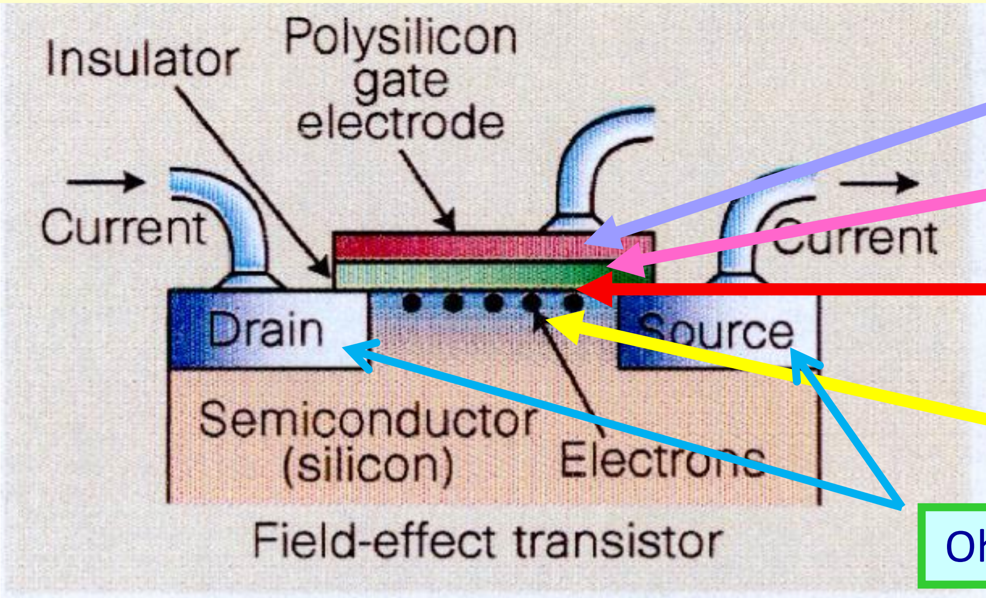
What are the next "Big Innovation(s)"?

Beyond CMOS – new physics and novel devices

- CMOS integrated circuit technology for computation at an inflexion point
  - The technology has enabled the semiconductor industry to make vast progress over the past 40 years.
  - It is expected to see the challenges going beyond the ten/twenty-year horizon.
    - Particularly from an energy efficiency point of view.
- Extremely important for the semiconductor industry/academic institutions to discover a new technology which will carry us to the beyond CMOS area
  - Power-performance of computing continues to improve
- New devices
  - Spintronics
  - Non-Boolean logic associated memory
  - Quantum computing

Device Scaling – Beyond Si CMOS:
high κ, metal gates, and high carrier mobility channel

1960 Kahng and Atalla, Bell Labs First MOSFET



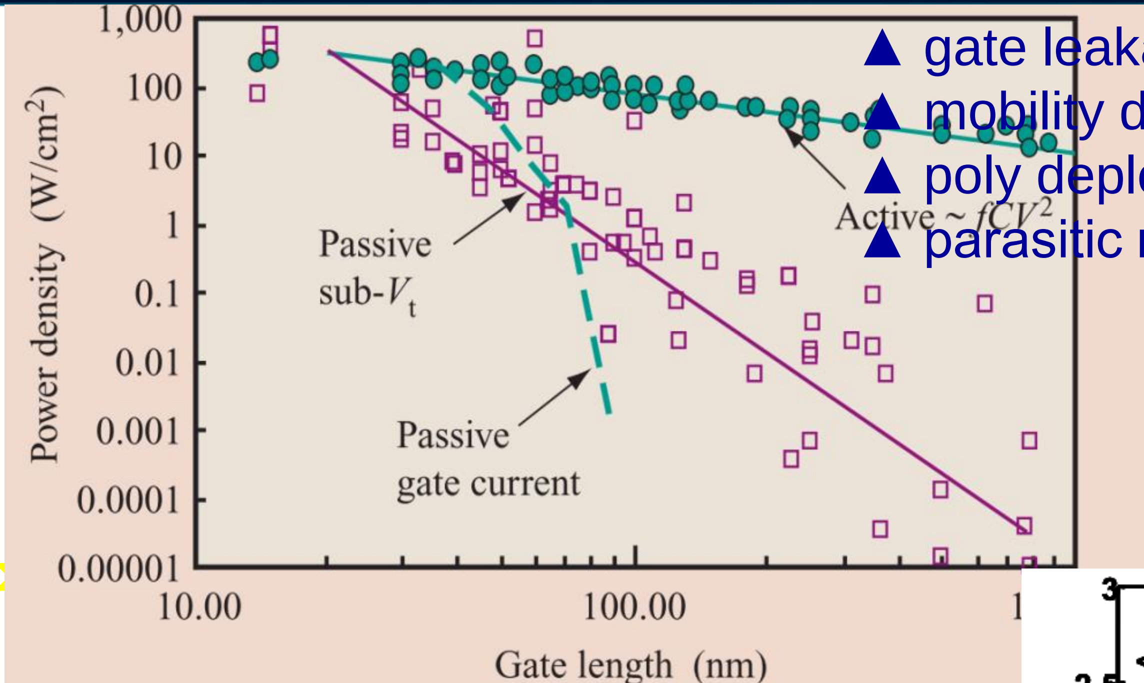
Integration of IIIV, Ge, GaN with Si

Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

Driving force :
High speed
Low power consumption
High package density

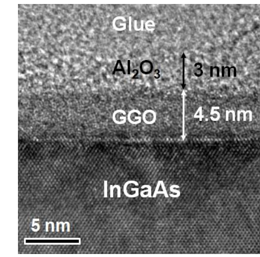
Why high-κ/III-V's?



W. Haensch *et al*., IBM J. Res. & Dev. **50,** 339 (2006)

- ▲ gate leakage
- ▲ mobility degradation
- ▲ poly depletion
- ▲ parasitic resistance …

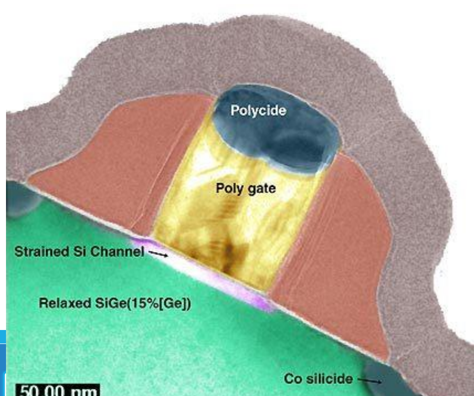
III-V



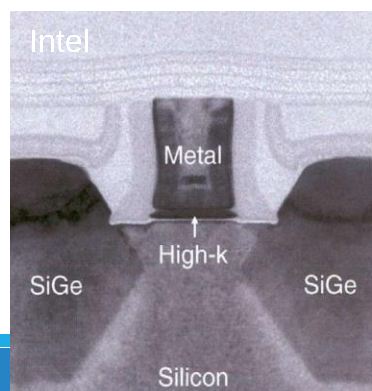
15nm
2014-2015

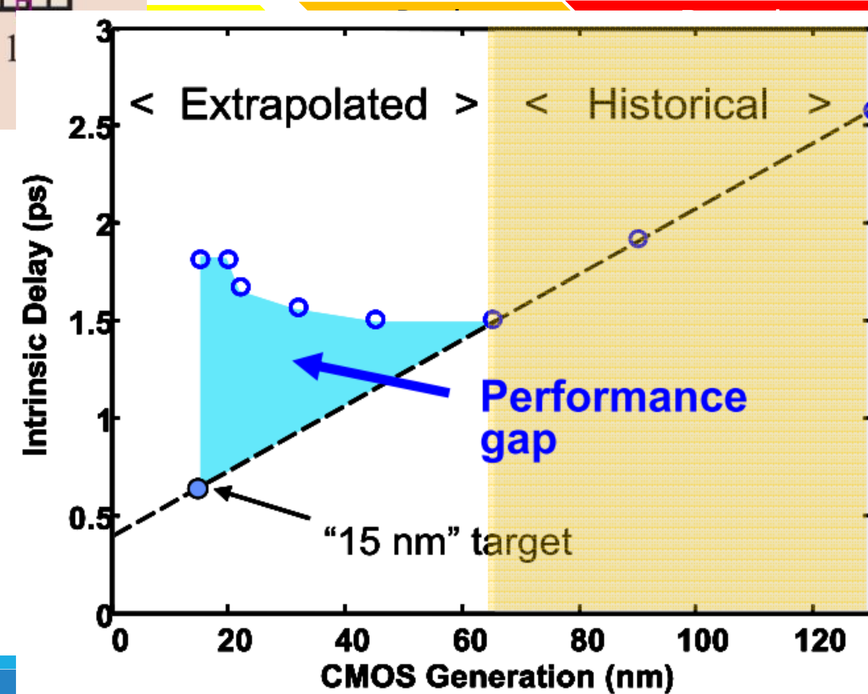
10--7nm
2014
… ?

Strained Si



High-κ metal Gate





D. Antoniadis, MIT

III-V Surface Passivation

Requirements

- *thermally and electronically stable at high temperatures of >800 ℃*
- *low leakage currents*
- *low interface trap density (D_{it})*
- *high κ values ⇒ low EOT < 1nm*

Early Efforts (1960s - 1990s)

reviewed by Hong et al, "Encyclopedia of Electrical and Electronics Eng.", v. 19, p. 87, Ed. Webster, John Wiley & Sons, 1999

- Anodic, thermal, and plasma oxidation of GaAs
- Wet or dry GaAs surface cleaning followed by deposition of various dielectric materials

1st Breakthrough (1994)

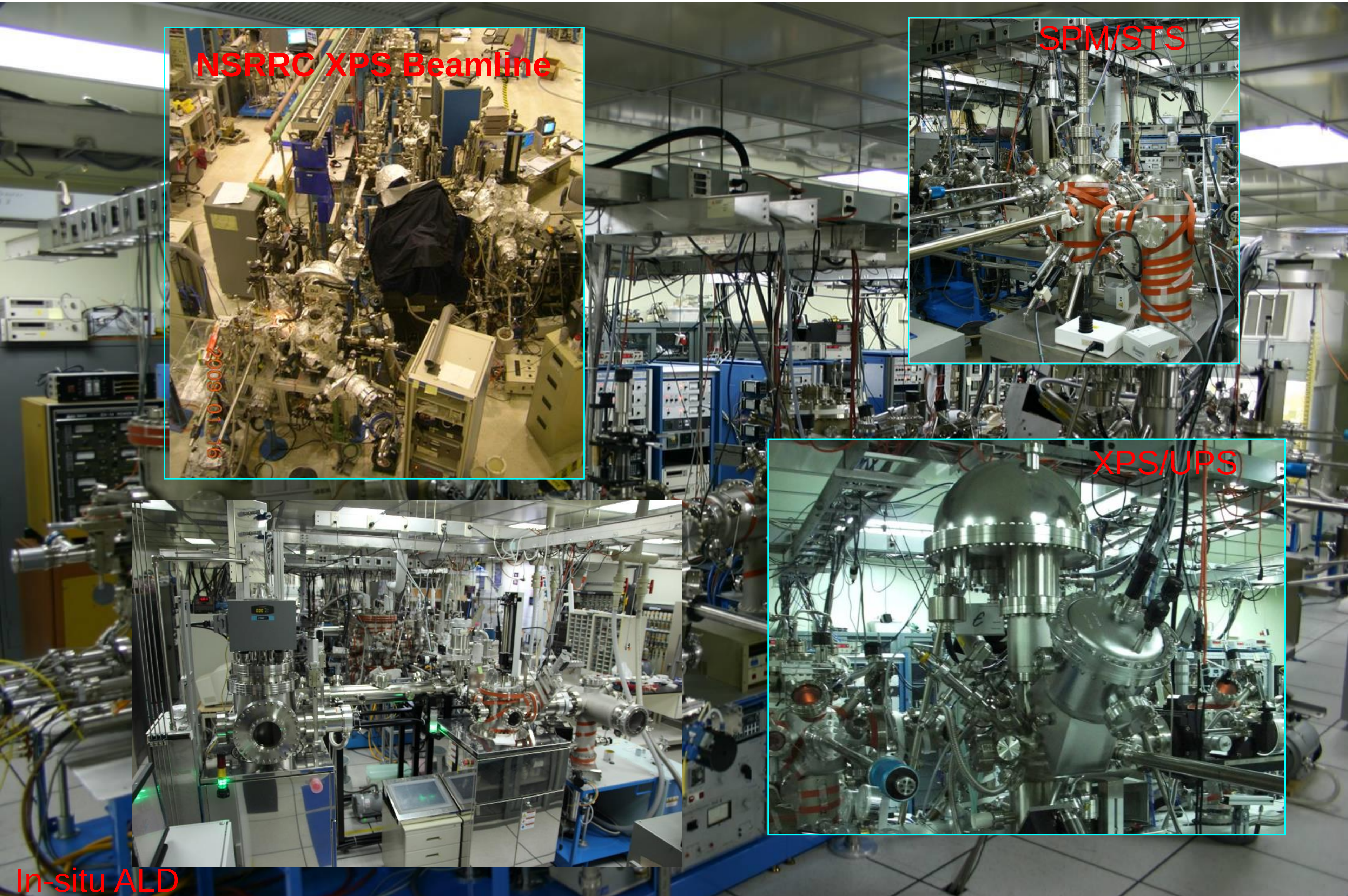
- ***in-situ*** **UHV deposited $Ga_2O_3(Gd_2O_3)$ [GGO] and Gd_2O_3 (Bell Labs)**

Hong, Kwo et al,
- JVST (1996);
- Science (1999)
- APL (1999)

Recent Demonstrations

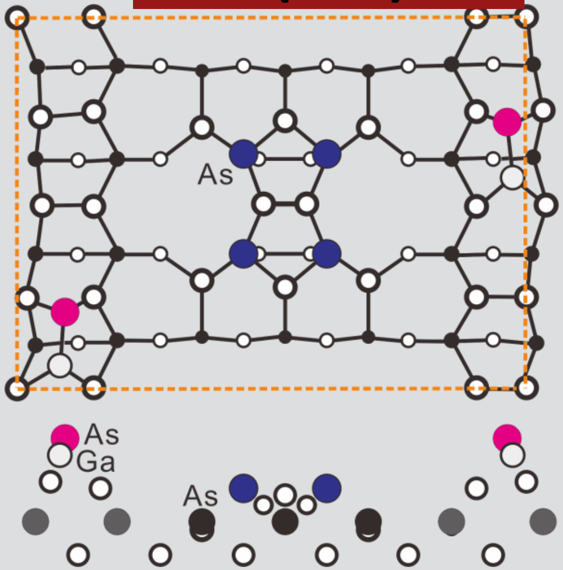
- ***in-situ*** **UHV deposited high-κ's** (NTU/NTHU, Freescale/U. Glasgow, IMEC, UT-Dallas …)
- ***ex-situ*** **ALD high-κ's** (Agere, Purdue U., NTU/NTHU, Intel, IBM, IMEC, UCSB…) **(2003)**
- **a-Si or Ge interfacial passivation layers (IPLs)+ high-κ's**

  (IBM, UT-Dallas, UT-Austin, NUS, U. Albany-SUNY/Intel/SEMATECH …)
- ***in-situ*** **ALD high-κ's** (NTU/NTHU, UTD) **(2009)**

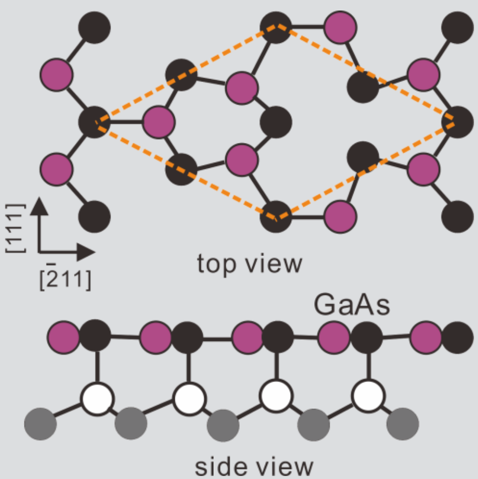

NSRRC XPS Beamline
2009 01 16
SPM/STS
XPS/UPS
In-situ ALD

atomic structure of (In)GaAs

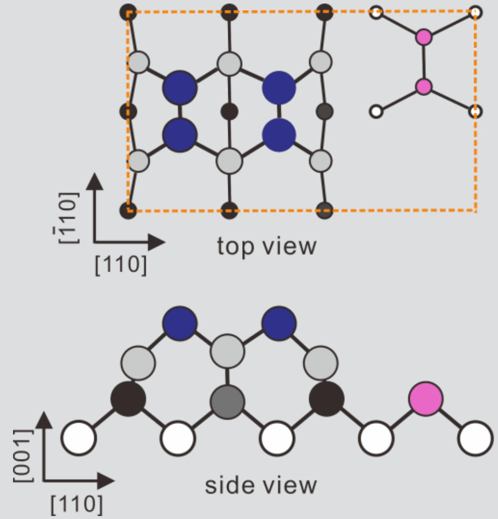
GaAs(001)-4x6



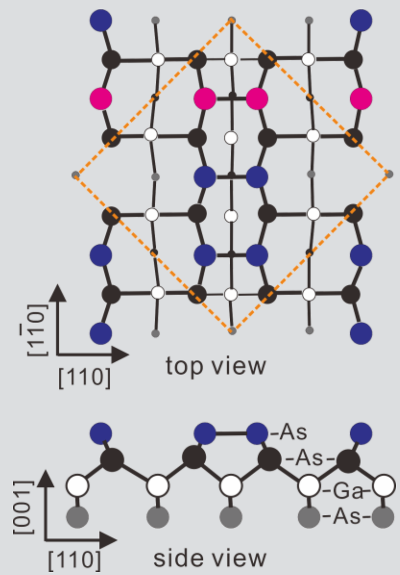
GaAs(111)A-2x2



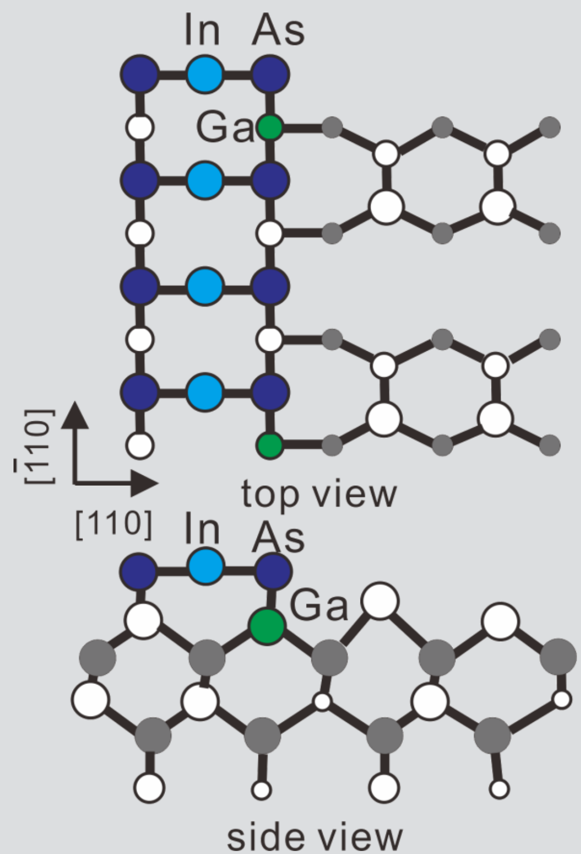
GaAs(001)-2x4



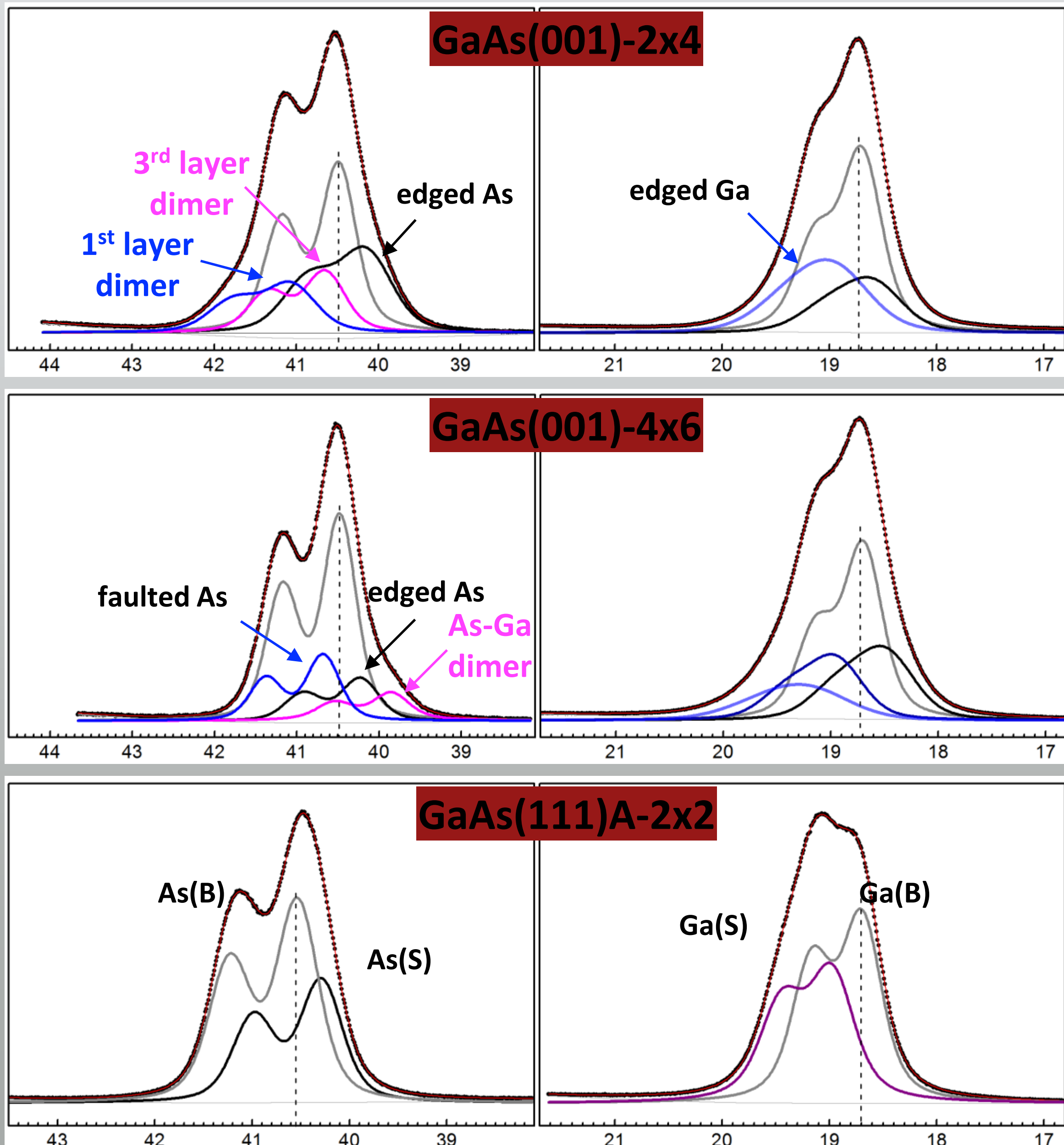
GaAs(001)c-4x4

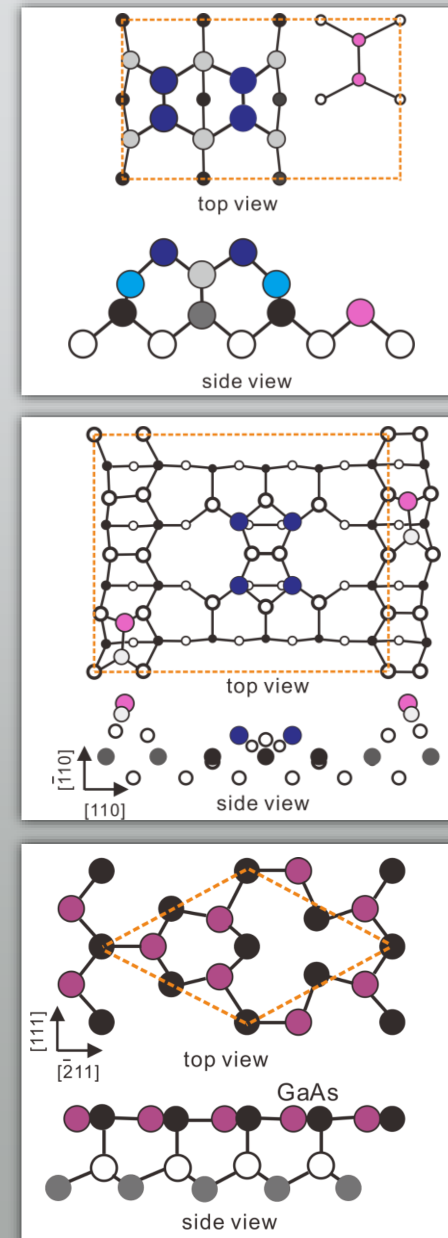


In_xGa_yAs(001)-4x2

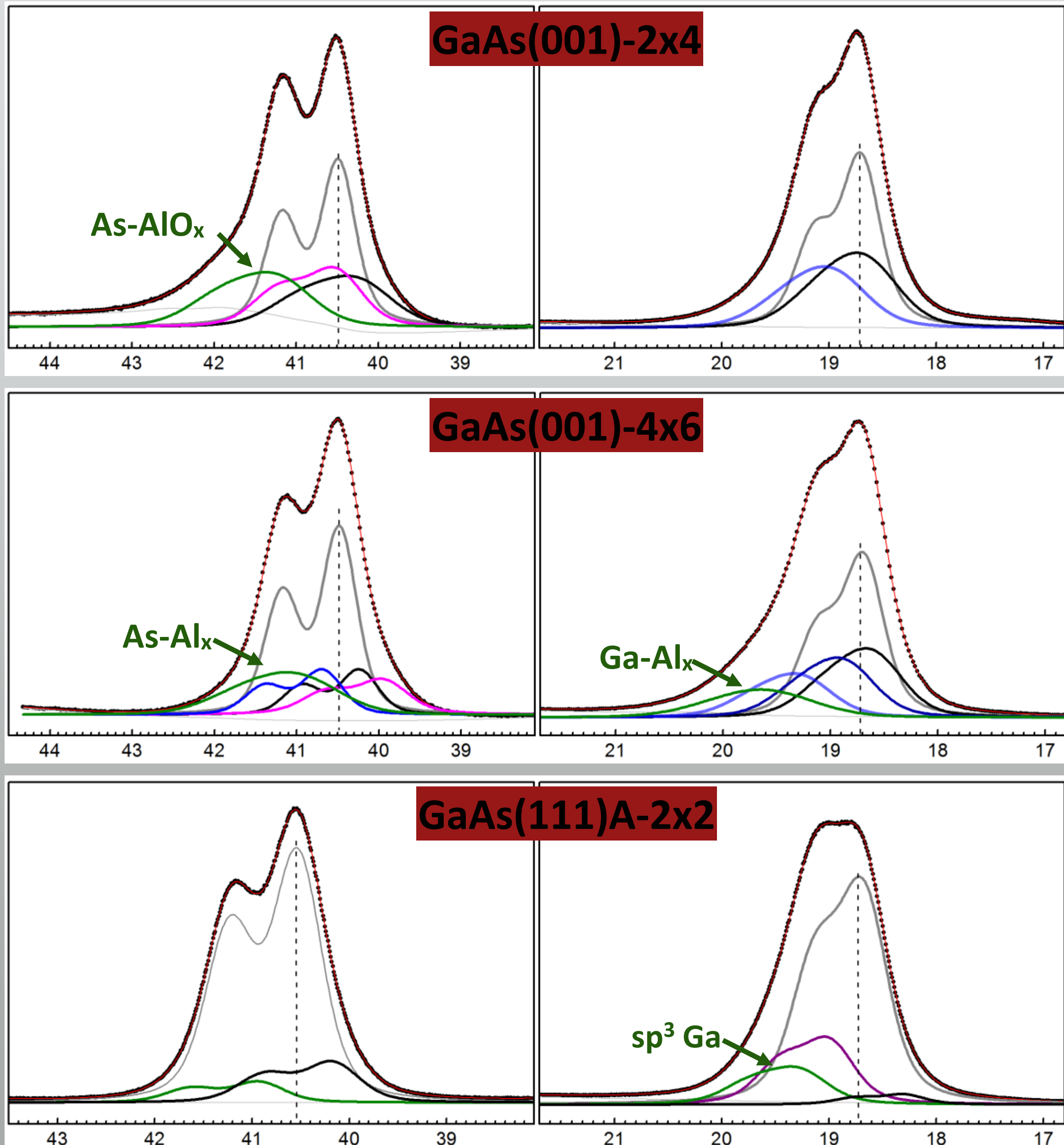


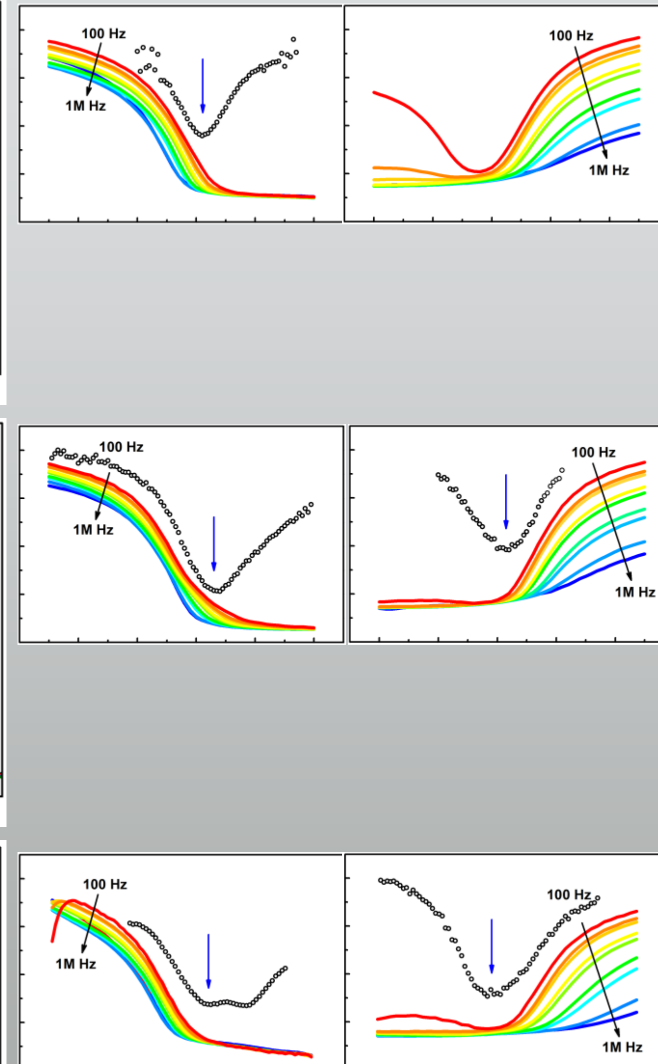
clean GaAs surfaces



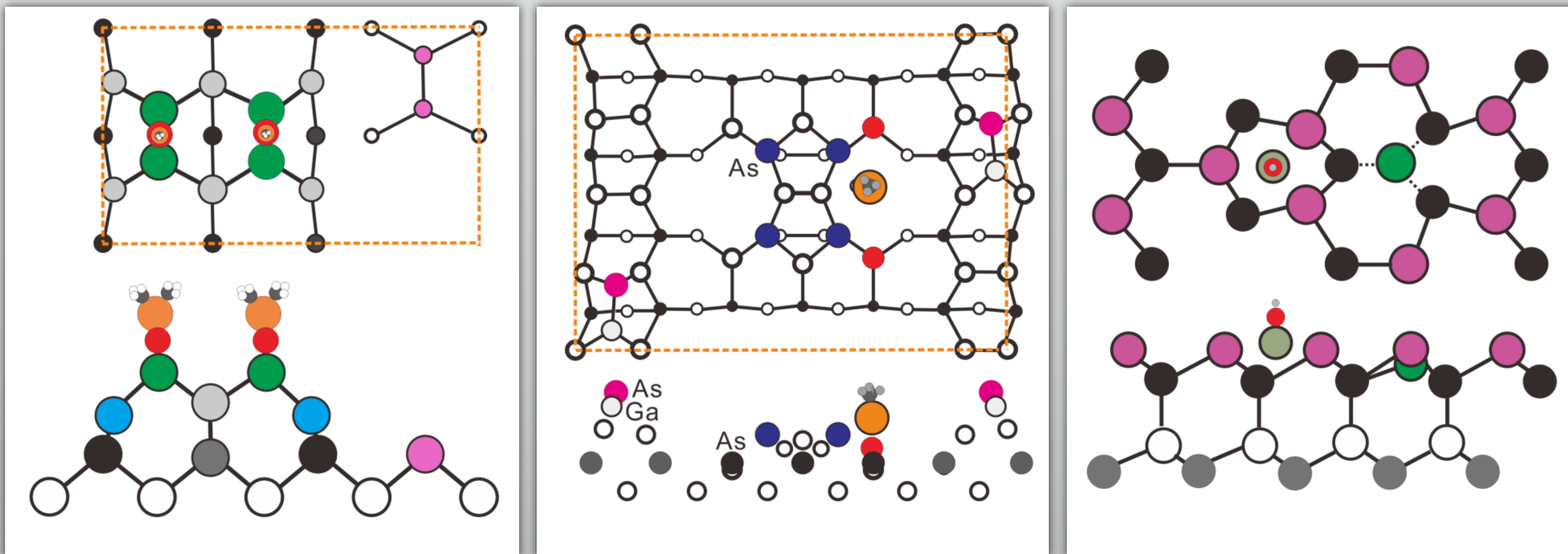


1 cycle of ALD (TMA+H_2O) on





ALD (TMA+H_2O) on GaAs



For GaAs(001)-2x4 and GaAs(001)-4x6:

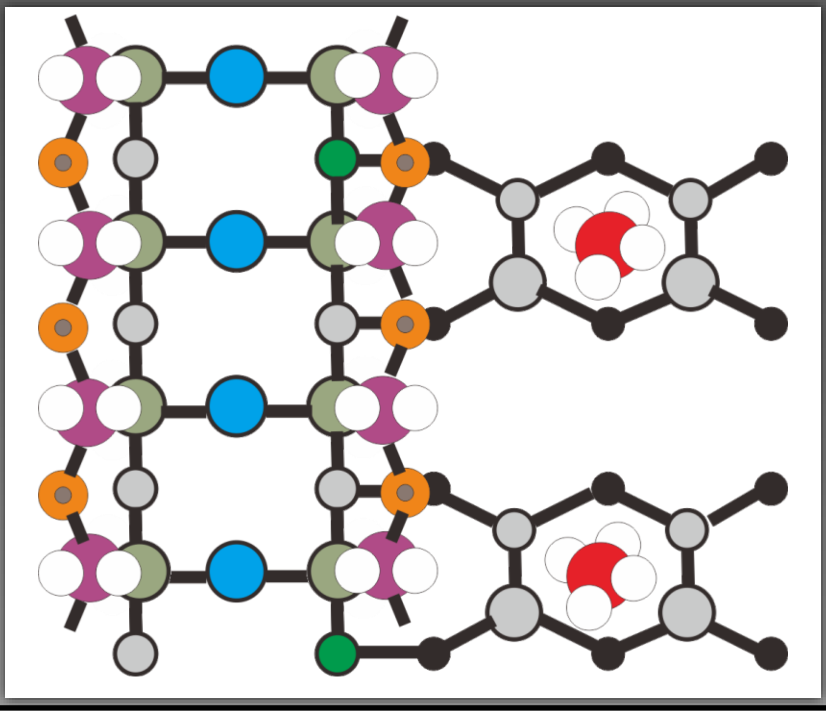
- The precursors attach partially the topmost As layer, leaving other surface atoms intact

For GaAs(111)A-2x2:

- Al sits at the the Ga-vacant site, thereby passivating the As dangling bonds
- The precursors relax the surface reconstruction, thus generating Ga dangling bonds

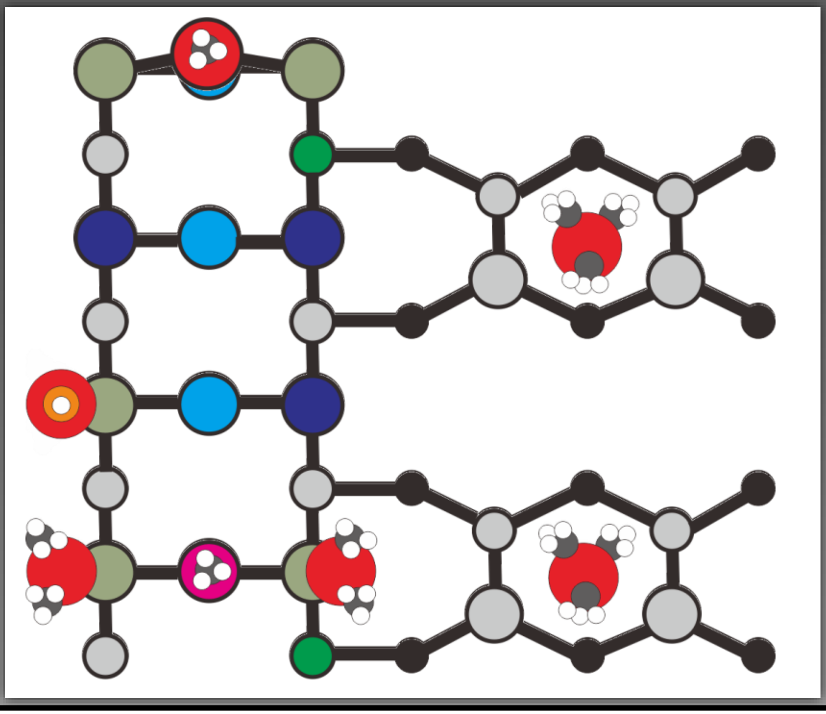
1 cycle of $(TMA+H_2O)/(TEMAHf+H_2O)$ on $In_xGa_yAs(001)$-4x2

$(TEMAHf+H_2O)$ on $In_{0.53}Ga_{0.47}As(001)$-4x2



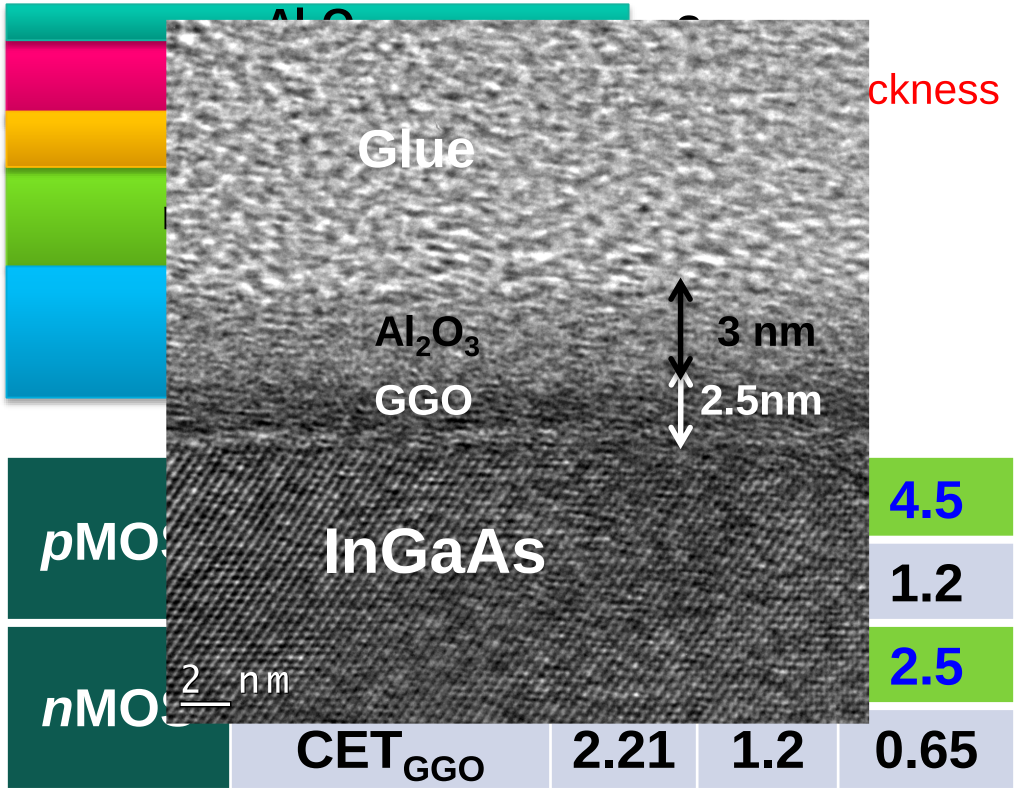
- Hf remains in the 4+ charge state
- All the top row As atoms are bonded with Hf
- The top row In atoms are not passivated
- Some top row In atoms are expelled

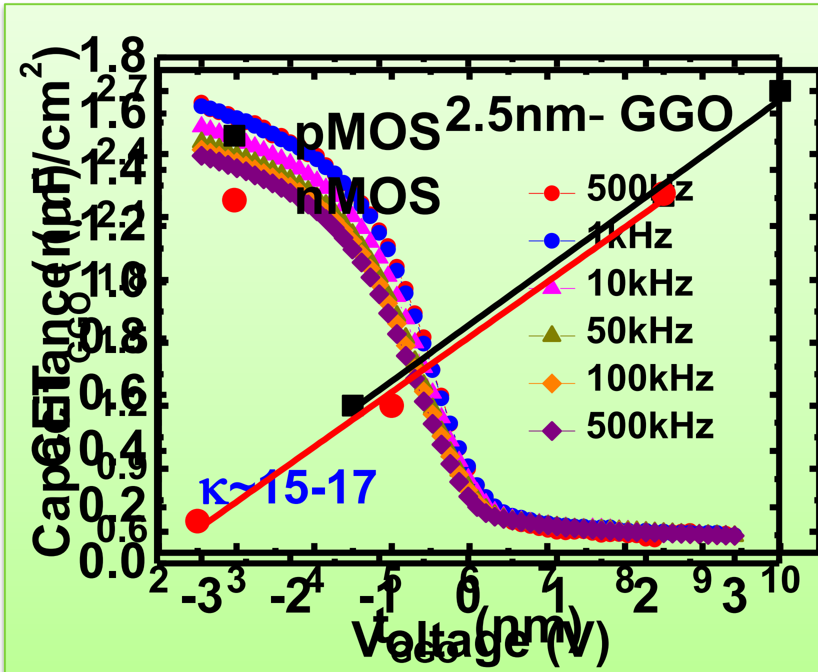
$(TMA+H_2O)$ on $In_{0.20}Ga_{0.80}As(001)$-4x2



- Al exists in TMA, DMA, and MMA
- DMA/MMA bonds with the top row As atoms
- The top row In atoms are not passivated
- 1 cycle passivates partially the row As

GGO Scalability and Thermal Stability





K. H. Shiu *et al.*, APL **92**, 172904 (2008)
T. H. Chiang *et al.*, unpublished

- Al_2O_3 capping effectively minimized absorption of moisture in GGO
- GGO (2.5nm) dielectric constant maintains ~15 (CET~7Å)
- D_{it}'s ~ low 10^{11}($cm^{-2}eV^{-1}$) range even subjected to 900°C annealing
  (Conductance Method)

Ultimate CMOS - $In_{0.53}Ga_{0.47}As$

Applications:

- **Optoelectronics in Optical communication and Photon sensor (Output value >30B USD in 2013, Annual growth rate >9%)**
- **High performance CMOS technology in logic circuit (Output value >300B USD, Annual growth rate >5% in 2013)**

Challenges:

- **$In_{0.53}Ga_{0.47}As$ surface passivation with tetra-valence high κ's is recognized as "MISSION IMPOSSIBLE"**
  →The importance of high k's/$In_{0.53}Ga_{0.47}As$ interface control is addressed
- **Low re-crystallization temp. of ~600°C for pure HfO_2 restricts the thermal budget for device processing**

Experiment and accomplishments:

✓ **ALD Hf-based high κ oxide is commercialized in Si CMOS industry**
→ Benefit from Mass Production and sufficiently high κ value

✓ **Clean and atomically ordered fresh $In_{0.53}Ga_{0.47}As$ surface w/o chemical treatment or interfacial passiv. layer**

✓ **Thin ALD-HfO_2 (0.8nm) initial layer followed by ALD-HfAlO top layer to enhance thermal stability (>800°C)**

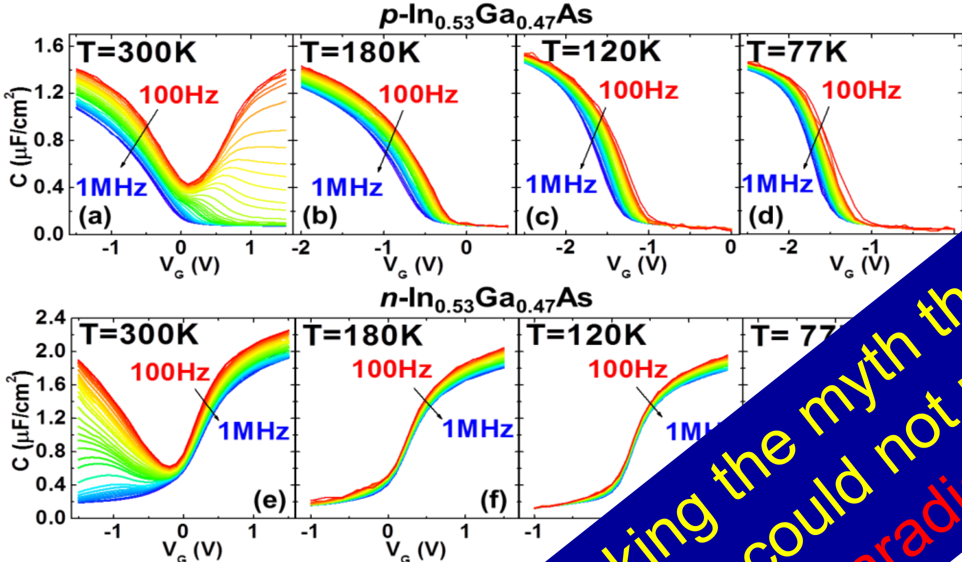
✓ **Best Interfacial Properties and MOS Devices Performance reported so far among the worldwide research groups**

Publication:
T. D. Lin, J. Kwo, and M. Hong et al., Appl. Phys. Lett. **100**, 172110 (2012)
T. D. Lin, J. Kwo, and M. Hong et al., Appl. Phys. Lett. **103**, 253509 (2013)

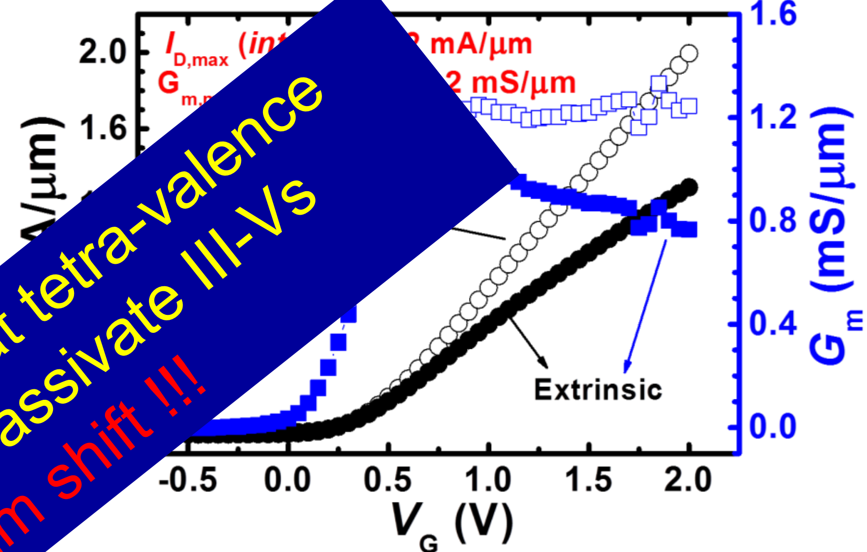
Ultimate CMOS – high k/$In_{0.53}Ga_{0.47}As$

Experiment Results:

ALD-HfAlO/HfO_2 (0.8nm)/$In_{0.53}Ga_{0.47}As$



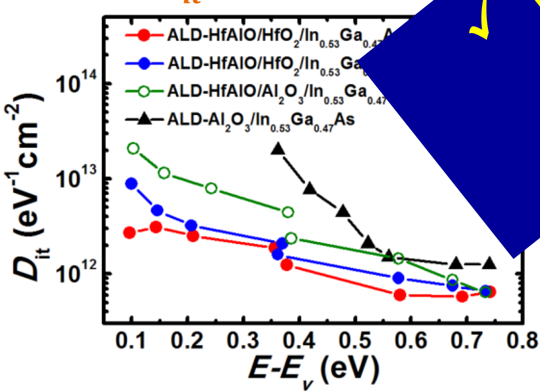
1 μm Lg Device performance

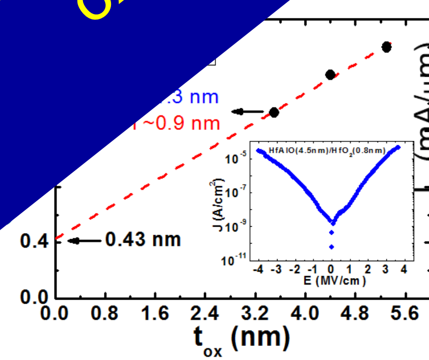


✓ Breaking the myth that tetra-valence oxide could not passivate III-Vs

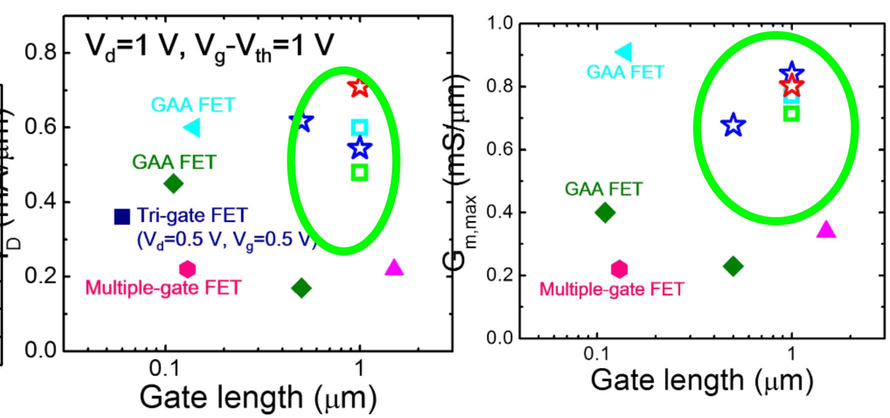
✓ Paradigm shift !!!

D_{it} distribution

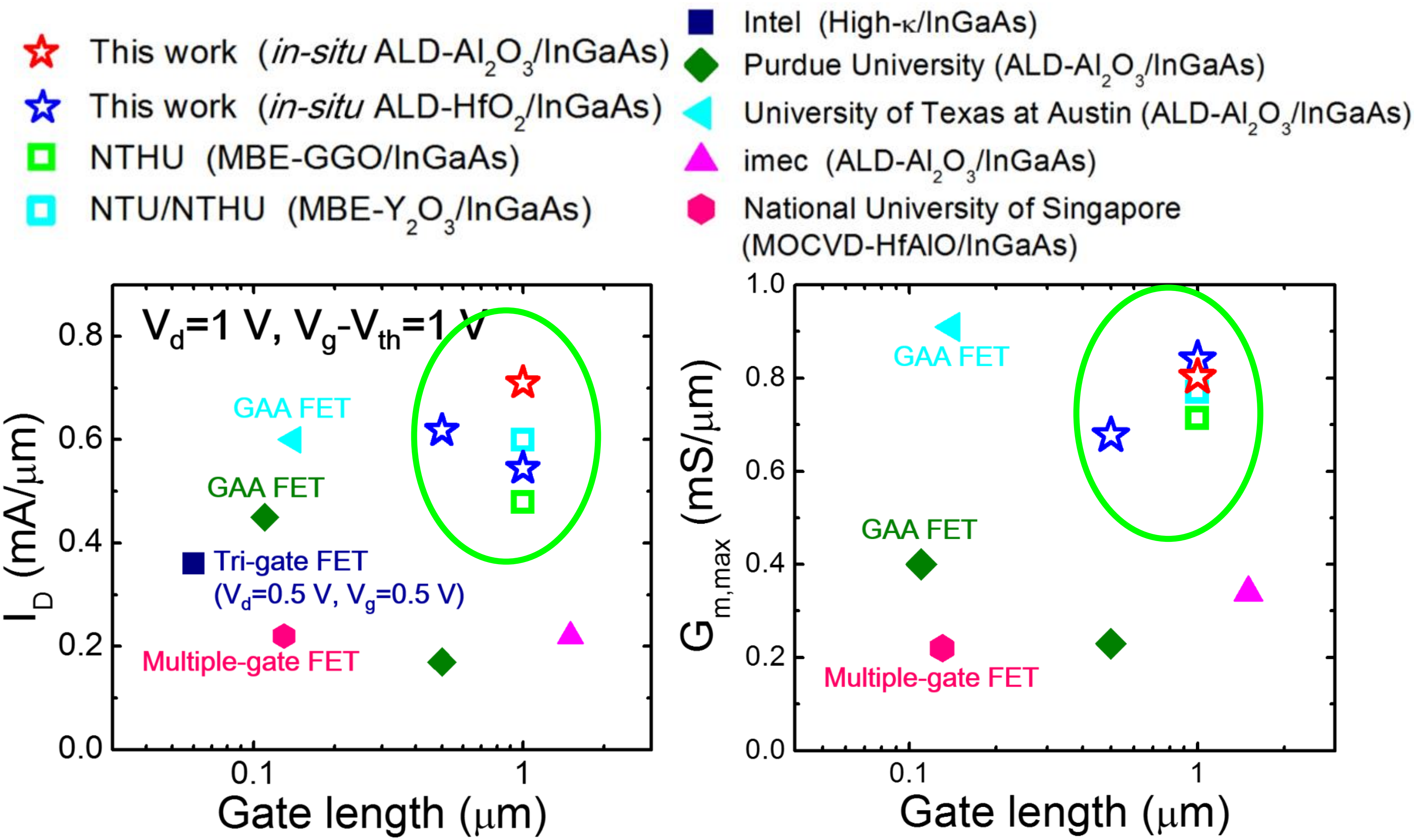




Benchmark



State-of-the-art InGaAs MOSFETs
Performance Benchmarking (extrinsic)



2012 International Technology Roadmap for Semiconductors (ITRS)

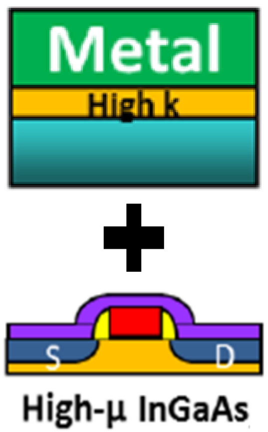
High-performance (HP) Logic Technology Requirements

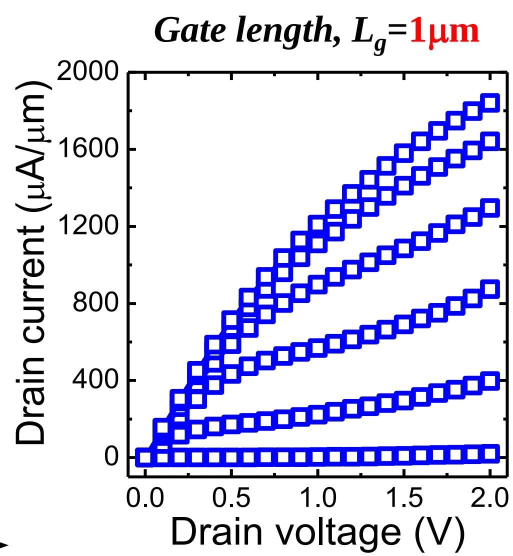
Year of Production	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**	**2025**	**2026**
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6.0
L_g: Physical Lgate for HP Logic (nm) [1]	**24**	**22**	**20**	**18**	**17**	**15.3**	**14.0**	**12.8**	**11.7**	**10.6**	**9.7**	**8.9**	**8.1**	**7.4**	**6.6**	**5.9**
$I_{d,sat}$: NMOS Drive Current (μA/μm) [14]																
Extended Planar Bulk	1,320	1,367	1,422	1,496	1,582	1,670	1,775									
FD SOI			1,475	1,530	1,591	1,654	1,717	1,791	1,847	1,942						
MG					1,628	1,685	1,744	1,805	1,858	1,916	1,976	2,030	2,087	2,152	2,228	2,308

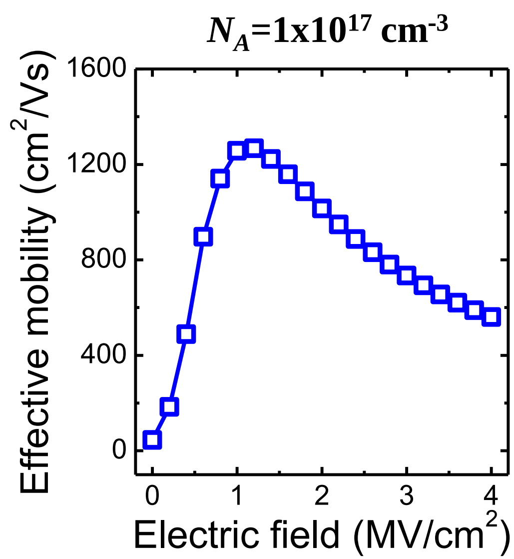
$I_{d,sat}$ > 1,800 μA/μm

http://www.itrs.net/Links/2012ITRS/Home2012.htm

High-κ/metal gate on high mobility III-V







Sheet resistance resulted in I_d degradation about 28% !
Contact resistance resulted in Id degradation about 9% !

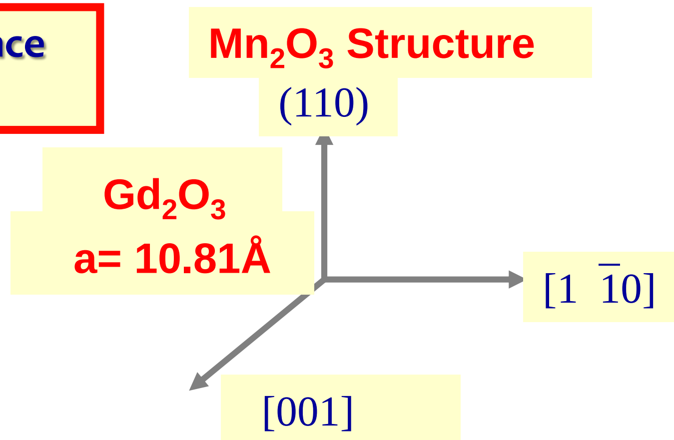
$I_{d,sat}$=**1840** μA/μm at V_d=2V Intrinsic Id > **2.6** mA/um

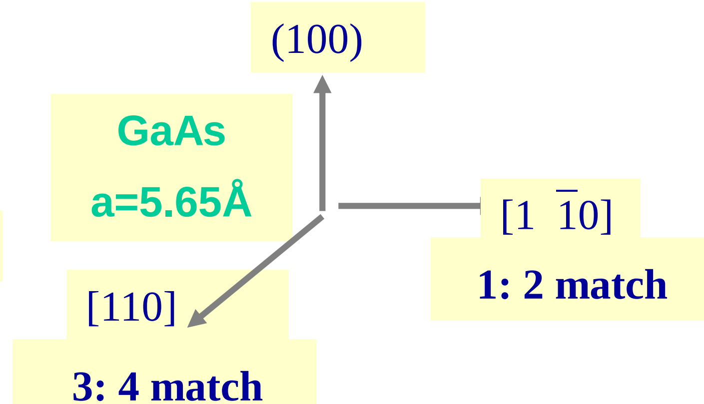
Effective mobility > **1200** cm²/Vs

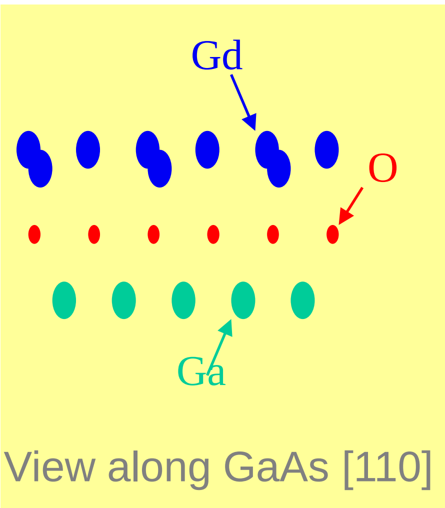
EOT ↓, L_g ↓ ➡ $I_{d,sat}$ ↑ at lower V_{dd}

Pioneer Work : Single Crystal Gd_2O_3 Films on GaAs

M. Hong, J. Kwo et al, Science 283, p.1897, 1999

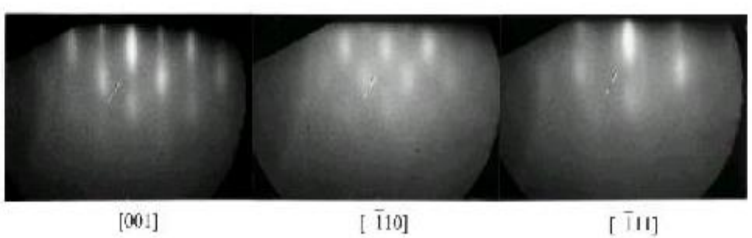


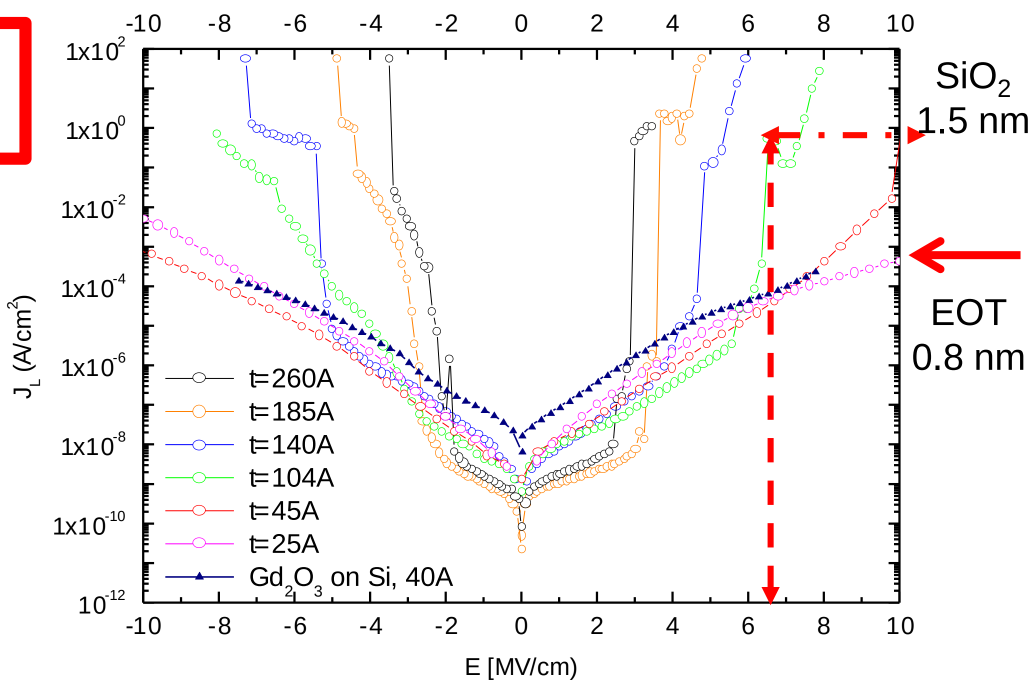




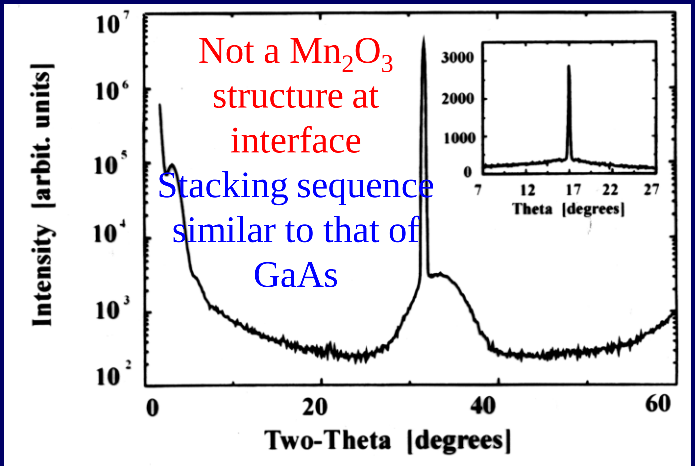
Low D_{it}'s and low J_L

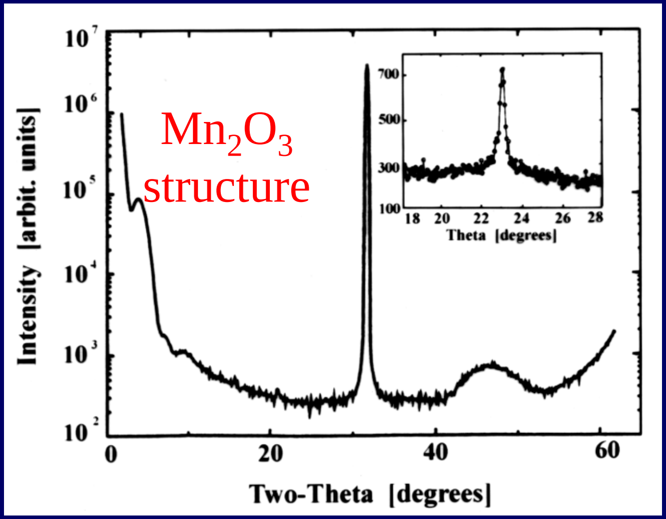
Gd_2O_3 (110) 25Å





Single crystal Gd_2O_3 on GaAs - Epitaxial interfacial structure

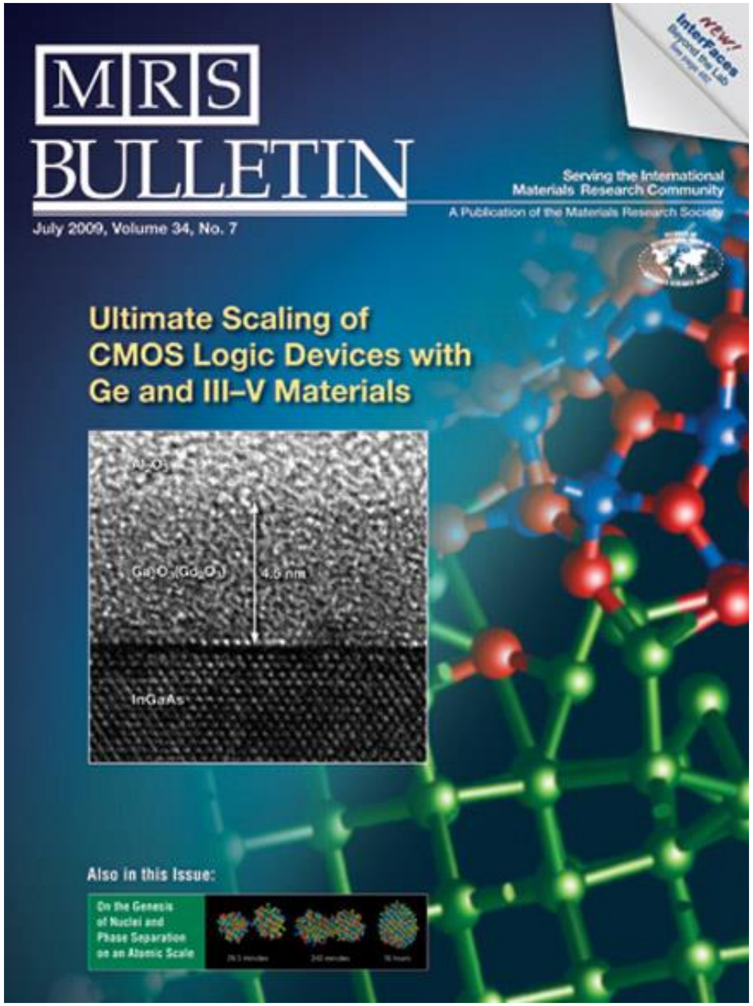


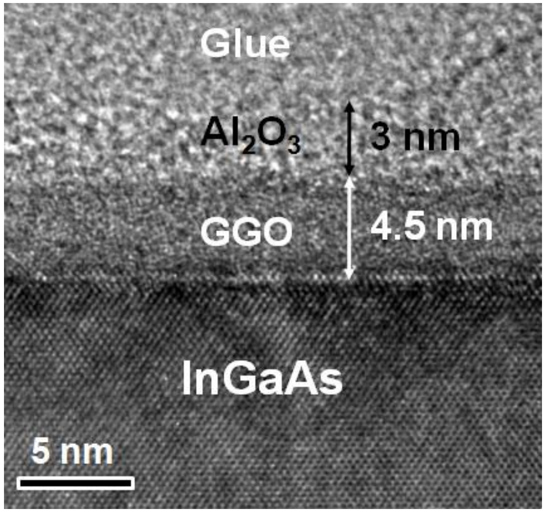


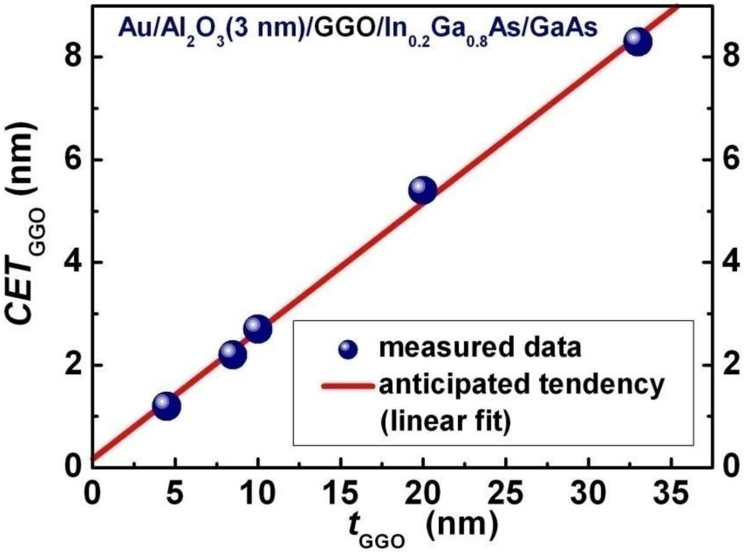
- "New Phase Formation of Gd_2O_3 films on GaAs (100)", J. Vac. Sci. Technol. B 19, 1434 (2001).
- " Direct atomic structure determination of epitaxially grown films: Gd_2O_3 on GaAs(100) " PRB 66, 205311 (2002)
- A new X-ray method for the direct determination of epitaxial structures, coherent Bragg rod analysis (COBRA)

→ Nature – Materials 2002 Oct issue cover paper

MRS Bulletin, July 2009





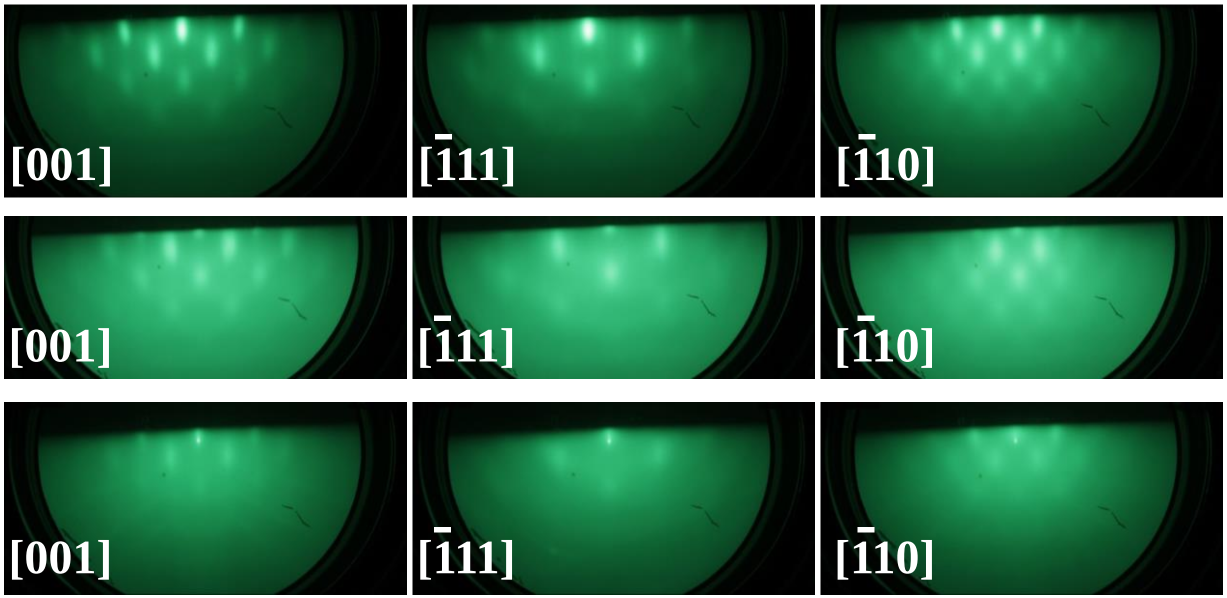


Cover Image & Theme Article – “*InGaAs Metal Oxide Semiconductor Devices with $Ga_2O_3(Gd_2O_3)$ High-κ Dielectrics for Science and Technology beyond Si CMOS*”, M. Hong, J. Kwo, T. D. Lin, and M. L. Huang, MRS Bulletin **34**, 514 July 2009.

K. H. Chen et al, poster

Growth monitored by RHEED

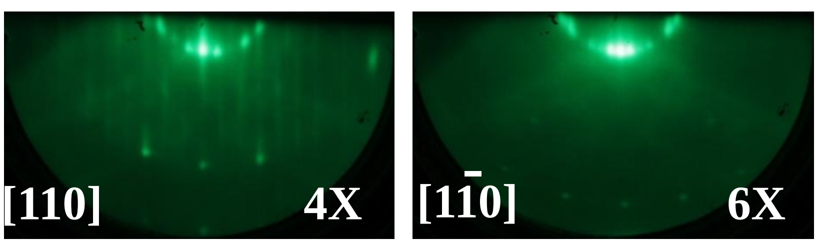
Single crystal ALD-Y_2O_3 was grown on GaAs(001)!!



5nm

2nm

1nm

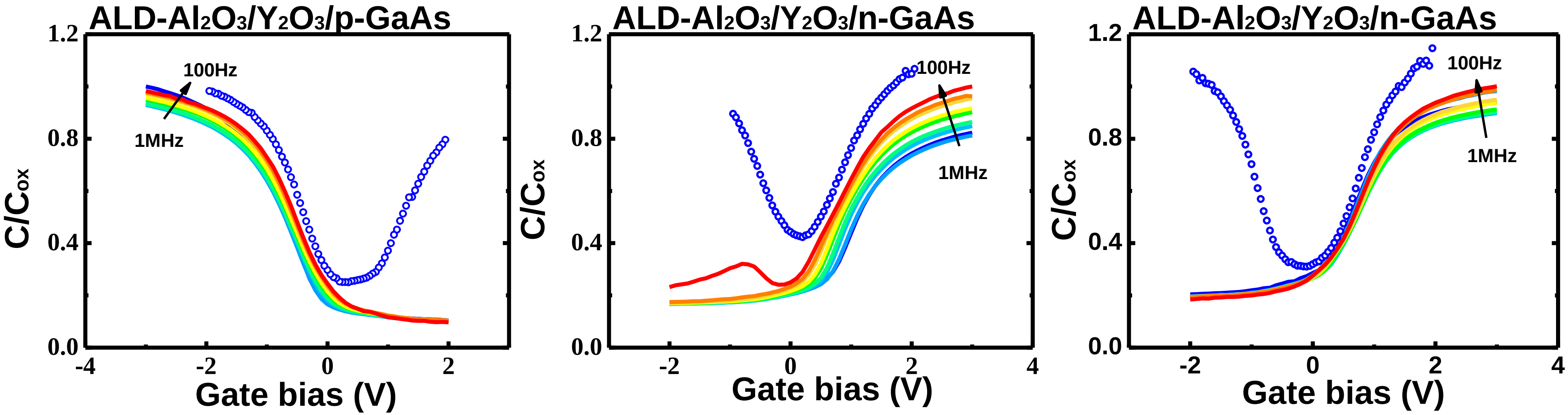


Freshly MBE-Grown GaAs surface

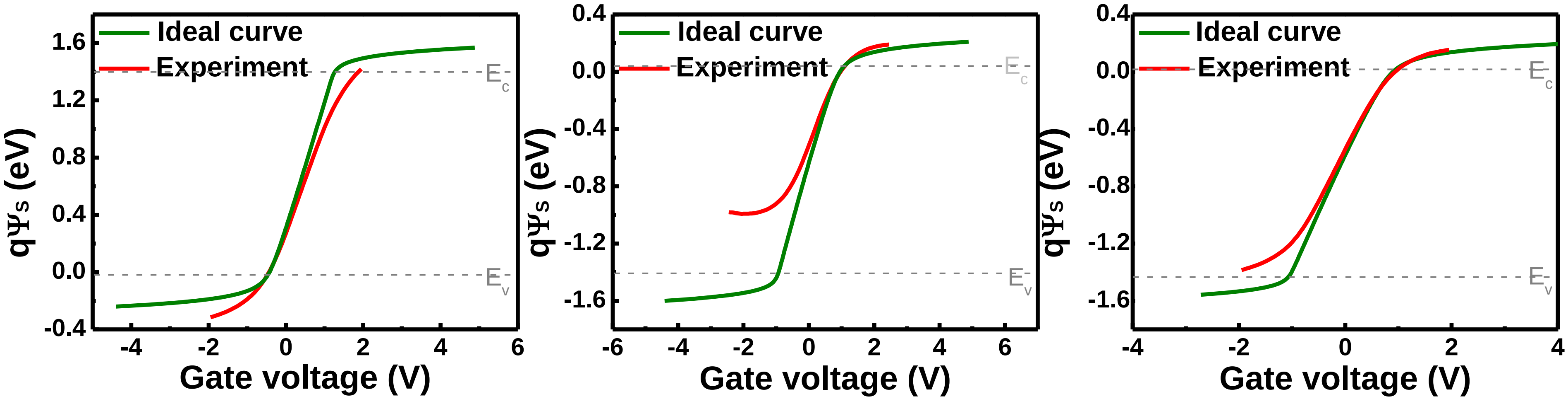
ALD-Y_2O_3

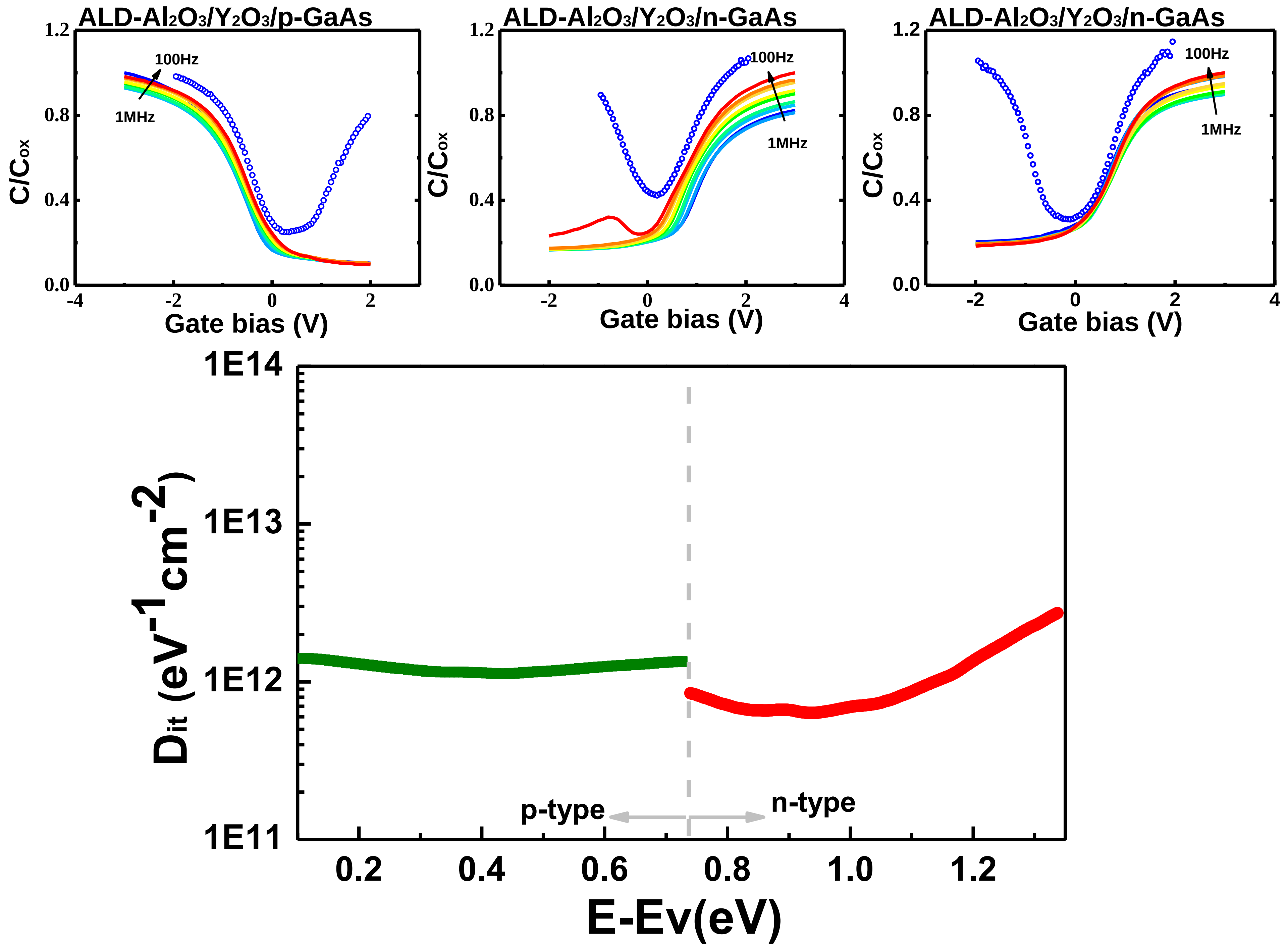
epi-GaAs

GaAs(001)



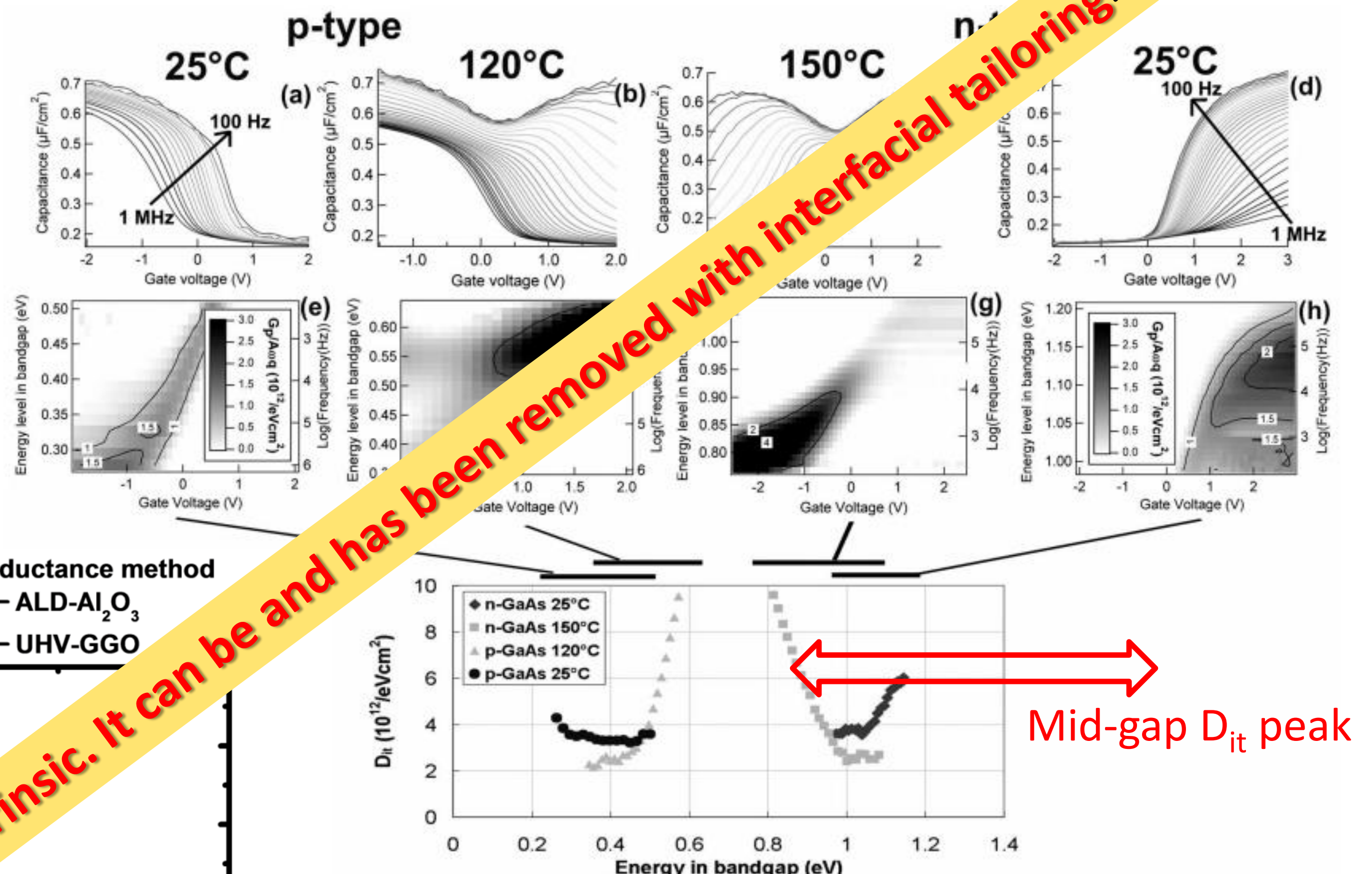
Surface potential vs. gate voltage

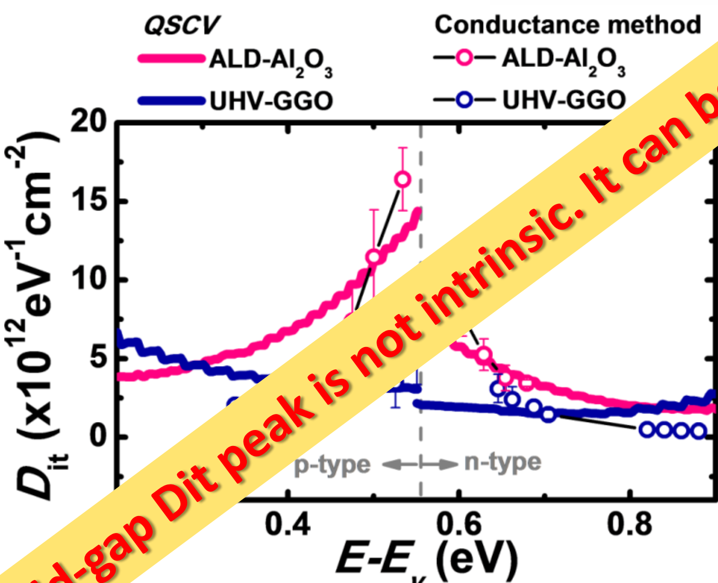




ALD-Al2O3/Y2O3/p-GaAs
ALD-Al2O3/Y2O3/n-GaAs
ALD-Al2O3/Y2O3/n-GaAs
100Hz
1MHz
C/Cox
Gate bias (V)
Dit (eV-1cm-2)
p-type
n-type
E-Ev(eV)

D_{it} spectrum for ALD-Al_2O_3/GaAs with HCl clean
(G. Brammertz *et al*, Appl. Phys. Lett. **93**, 183504 (2008))





Mid-gap Dit peak is not intrinsic. It can be and has been removed with interfacial tailoring.

C. A. Lin & H.C. Chiu *et al.*, *APL* 98, 062108 (2011)

Summary – Grand Accomplishments and Challenges

- Perfecting the best atomic-scale hetero-structures and their interfaces in high κ and high carrier mobility semiconductors of InGaAs, Ge, (In)GaSb, GaN
- Probing them with the most powerful analytical tools (XPS and x-ray diffraction using synchrotron radiation, *in-situ* XPS, STM/STS, and HR-TEM)
- Producing novel, high-performance electronic devices ready for **ultimate CMOS**
- **Innovations involving quantum mechanics and spin**
  - **Spintronics**
- **Further reduce frequency dispersion at accumulation for high k/semiconductors**
- **Greatly reduce interfacial trap densities and border traps**
- **Greatly reduce CV hysteresis**
- **Understanding and tailoring Schottky barrier heights**